**In the Claims:**

Please amend the claims as follows:

1.(Amended) A method of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer; [and]

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer;

subsequently etching said bottom electrode layer.

2.(Amended). The method of claim 1, further comprising forming a non-insulating layer over at least a portion of the resultant structure subsequent to forming said conformal insulating layer and prior to etching said bottom electrode layer.

3.(Amended) A [The] method of [claim 2,] forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer,

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said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer; and

forming [wherein said non-insulating layer is] an anti-reflective layer (ARL) over at least a portion of the resultant structure subsequent to forming said conformal insulating layer.

4.(Amended) A [The] method [according to claim 3,] of forming a capacitor in an integrated circuit comprising:

forming a bottom electrode layer on a semiconductor body;

forming a dielectric layer over at least a portion said bottom electrode;

forming a top electrode layer over at least a portion of said dielectric layer;

removing a portion of said top electrode layer to expose a portion of the dielectric layer;

subsequently removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said lower electrode layer;

subsequently forming a conformal insulating layer over at least a portion of said exposed portion of the bottom electrode layer proximate to said exposed dielectric layer, said exposed dielectric layer and at least part of said top electrode layer proximate to said exposed dielectric layer; and

forming [wherein said non-insulating layer is] an anti-reflective layer (ARL) over at least a portion of the resultant structure subsequent to forming said conformal insulating layer, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

Please add the following new claims:

--31.(New) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure, comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

and

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forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

32.(New) The method of claim 31, further comprising forming a non-insulating layer over at least a portion of the resultant structure subsequent to forming said conformal insulating layer.

33.(New) The method of claim 32, wherein said non-insulating layer is an anti-reflective layer (ARL).

34.(New) The method according to claim 33, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

35.(New) The method according to claim 32, wherein said bottom electrode layer is additionally used to form the gate of one or more transistors formed in said integrated circuit.

36.(New) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

forming a capacitor structure comprising:

a top electrode over a portion of said conductive layer; and

a dielectric layer between said top electrode and said conductive layer;

forming a conformal insulating layer over said capacitor structure and at least a portion of said conductive layer proximate to capacitor structure;

forming an anti-reflective layer (ARL) over at least a portion of the structure resultant from said forming a conformal layer;

forming a patterned mask over the structure resultant from said forming an ARL; and

etching said conductive layer using said patterned mask.

37.(New) The method according to claim 36, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

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38.(New) The method according to claim 37, wherein said conformal insulating layer is an oxide layer is formed in a thermal process.

39.(New) The method according to claim 36, wherein said conductive layer is additionally used to form the gate of one or more transistors formed on said integrated circuit.

40.(New) A method of forming an integrated circuit comprising:

forming a conductive layer on a semiconductor body;

providing a process flow for etching said conductive layer, whereby the gates of one or more transistors are formed, said flow including a photolithographic process comprising:

forming an anti-reflective layer (ARL) over at least a portion of the conductive layer; and

forming a patterned mask over said ARL, wherein said photolithographic process is optimized for forming said gates;

performing a capacitor formation process comprising:

forming one or more capacitor structures, each comprising a top electrode over a portion of said conductive layer and a dielectric layer between the top electrode and the conductive layer; and

forming a conformal insulating layer over said capacitor structures and at least a portion of said conductive layer proximate to capacitor structures, wherein the capacitor formation process is performed prior to forming said ARL, whereby said ARL is additionally formed over said capacitor structures, and whereby said conformal insulating layer is formed such that said provided process flow is unaltered; and

etching said conductive layer according to said process flow, whereby the lower electrodes of said capacitor structures and said gates are formed.

41.(New) The method according to claim 40, wherein said conformal insulating layer has a thickness in the range of from 20Å to 70Å.

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